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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,182	10/02/2003	Jee-Soo Mok	LEPA121687	8329

26389 7590 01/03/2008

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EXAMINER	
AHMED, SHAMIM	
ART UNIT	PAPER NUMBER
1792	

MAIL DATE	DELIVERY MODE
01/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/677,182	MOK ET AL.	
	Examiner	Art Unit	
	Shamim Ahmed	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-15 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-15 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/30/07 has been entered.

Response to Arguments

2. Applicant's arguments filed 10/30/07 have been fully considered but they are not persuasive. Applicants argue that Kamayachi et al does not teach laminating a semi-cured film.

In response to the argument , examiner states that the argument is not persuasive because Kakayachi et al's deposited thermosetting resin dry film (semicured) is nothing but a laminate with the circuit board (col.15, lines 67-col.16, lines 1-5).

3. Applicants also argue that ordinary skilled in the art would not recognize that drying and semi-curing is the same thin as examiner discusses in the previous rejection and trying to support with Hayai (5,837,355) and additionally, applicants state that dry and semi-cure are distinct alternatives, not the same thing.

In response to the argument examiner states that the primary reference, Kamayachi et al disclose that the photosensitive thermosetting resin composition was

applied to the entire surface of a copper through-hole printed circuit board with a roll coater (product of The Pilot Seiko Co., Ltd.). The board coated with the resin composition was placed in a hot air circulation oven, dried therein at 80.degree. C. for 20 minutes, and then left cooling to room temperature, to produce a board with a dry coating (col.19, lines 54-65).

And Hayai discloses that heating is applied to the thermosetting resin to dry or semi-cure the resin in which the heating is considered to be semi-curing the resin and both the heating and the semi-curing are similar process or functionally equivalent process for the thermosetting resin material.

Therefore, the previous rejection is repeated herein as follows:

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1, 3-15 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamayachi et al (4,943,516) as supported with Hayai (5,837,355) in view of Paulus (5,626,774) and further in view of Applicant's admitted prior art (AAPA).

Kamayachi et al disclose a process of forming a solder resist pattern on a printed circuit board (col.1, lines 7-20), wherein the process including the steps of:

- Laminating or depositing a thermosetting resin film on a printed circuit board (PCB) having circuits formed thereon, wherein the resin can be in a wet or dry state (semi-cured), wherein the dry film is semi-cured thermosetting film, which is supported by Hayai (5,837,355).

Hayai discloses a multilayer printed circuit board comprises an interlayer circuit board laminated to a prepreg. A thermosetting epoxy resin coating is applied to at least one side of an interlayer circuit board having a circuit formed on at latest one side. The coating composition contains dicyandiamide and a micro-encapsulated imidazole compound. The applied coating is heated to dry or semi-cure the coating and the prepreg is laid on the dried or semi-cured coating and laminated to it (see the abstract).

- The coating is then directly exposed to a laser beam through a photomask having a prescribed pattern;
- Post-curing the developed thermosetting resin pattern to form solder resist pattern (col.15, line 67-col.16, line 31).

Kamayachi et al fail to teach the thermosetting resin film is selectively removed to remove the resin film according to prescribed solder resist pattern.

However, Paulus discloses a process of forming solder resist mask on the surface of a multilayered printed circuit board, wherein both side of a copper foil is laminated with a partially cured thermosetting resin, which is then irradiating or ablated with laser through an etch resist mask to remove selectively (col.1, lines 62-col.2, lines 14 and col.3, lines 5-11).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of claimed invention to employ paulus's teaching into Kamayachi et al's process for selectively removing the resin film according to a desired pattern.

Modified Kamayachi et al remain silent about the pre-treating the printed circuit board before lamination step.

However, Applicant's admitted prior art (AAPA, herein after) teach pre-treating such as scrubbing process is carried out on both sides of the substrate to improve the adhesion between the photo solder resist (PSR) and the substrate (see specification page 6, lines 8-10).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of claimed invention to combine AAPA's teaching into modified Kamayachi et al's process for increasing bonding capability between the circuit board substrate and polymeric solder resist material as taught by AAPA.

As to claims 23-24, Paulus also illustrate that typically printed circuit board (PCB) is formed four layered and the fabrication begin with forming circuits on both sides of the

laminated epoxy resin and inner circuits are shown connected to a second set of circuit by blind vias and finally, two substrates are laminated with heat and pressure to form multilayered printed circuit board (col.2, lines 52-col.3, lines 11).

7. Claims 1,3-15 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urasaki et al (5,879,568) in view of Paulus (5,626,774) and further in view of Applicant's admitted prior art (AAPA).

Urasaki et al wherein the process including the steps of:

- depositing a thermosetting resin on a printed circuit board (PCB) having circuits formed thereon, wherein the resin can be cured by heating (col.2, lines 61-col.3, line 2).
- the resin layer is then selectively irradiating with a laser beam in order to form prescribed solder resist pattern, wherein the types of laser includes carbon dioxide laser, YAG laser or excimer laser (col.7, lines 50-58 and col.9, lines 49-col.10, lines 57).

Urasaki et al fail to teach the thermosetting resin film is selectively removed to remove the resin film according to a solder resist pattern.

However, Paulus discloses a process of forming solder resist mask on the surface of a multilayered printed circuit board, wherein both side of a copper foil is laminated with a partially cured thermosetting resin, which is then irradiating or ablated with laser through an etch resist mask to remove selectively (col.1, lines 62-col.2, lines 14 and col.3, lines 5-11).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of claimed invention to employ Paulus's teaching into Urasaki et al's process for selectively removing the resin film according to a desired pattern using the pattern solder mask

Modified Urasaki et al also disclose that coating the thermosetting resin on the copper surface, wherein the copper surface having an appropriate roughness for bonding with the resin layer, which is then semi-curing by heating (col.6, lines 26-36) But fail to explicitly teach the pre-treating the printed circuit board before lamination step.

However, Applicant's admitted prior art (AAPA, herein after) teach pre-treating such as scrubbing process is carried out on both sides of the substrate to improve the adhesion between the photo solder resist (PSR) and the substrate (see specification page 6, lines 8-10).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of claimed invention to combine AAPA's teaching into Urasaki et al's process for increasing bonding capability between the circuit board substrate and polymeric solder resist material as taught by AAPA.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shamim Ahmed whose telephone number is (571) 272-1457. The examiner can normally be reached on Tu-Fri (12:30-10:30) Every Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Shamim Ahmed
Primary Examiner
Art Unit 1792

SA
December 31, 2007